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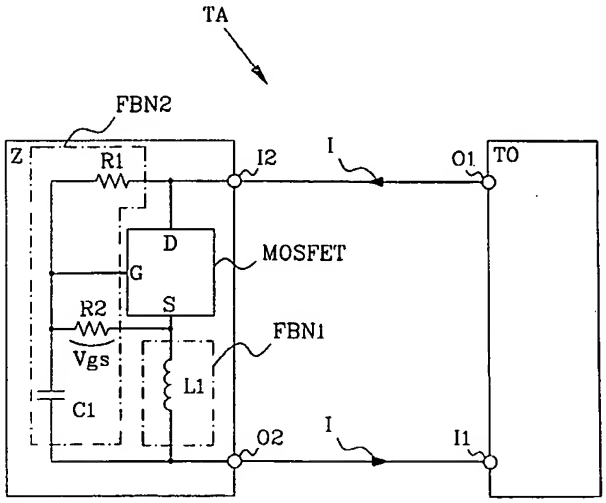
(54) Title: ACTIVE LOAD ARRANGEMENT



(57) Abstract: The present invention relates to an active load arrangement Z used to provide proper output load to an object TO under test. The arrangement Z comprises a voltage controlled transistor MOSFET having a source S, a gate G and a drain D. The drain D is associated with the gate G and connected to an arrangement input I2 associated with an output O1 of the object under test. The source S is connected to an arrangement output O2 associated with an input I1 of the object under test. A feedback arrangement is connected to the source S and the gate G. The feedback arrangement changes phase and amplitude of the gate-to-source voltage by varying frequency in order to obtain low impedance at low impedance at low frequencies and high impedance at high frequencies.

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ACTIVE LOAD ARRANGEMENT

TECHNICAL FIELD OF THE INVENTION

The present invention relates to an active load arrangement providing proper output load to a device under test.

DESCRIPTION OF RELATED ART

Automatic test equipment is frequently employed to run diagnostic tests on integrated circuit devices. A purpose of a testing device is to ensure that integrated circuits under test provide the proper output voltages given the input stimulus of the tester. It is necessary that such devices simulate the proper output load. In the US patent US 4,712,058 is disclosed an active load network for a device under test and for turning on either a current source or a current sink to properly load its output. The current sink and current source each comprises a pair of CMOS transistors connected in series. An active load network that provides low resistance for direct current DC and high impedance for alternating current AC is often necessary when testing an object of for example line interface type. This type of load network prevents superposed AC parameters to be essentially influenced by DC load. When measuring AC parameters of a test object, the AC impedance of the load network must be essentially higher than the AC impedance of the test object. High AC impedance and low DC resistance can be accomplished by an inductance. However, when measuring on low frequency signals from about 200 Hz and high impedance load above 150 kohm is required, the inductance has to be more than 120 H. This type of AC impedance is necessary when measuring for example on line interface circuits within POTS (Plain Old Telephone Service) telephony. A passive inductance i.e. a

coil of that inductance size which can stand enough current without being saturated will be bulky and expensive. The necessary size of such a coil may cause other types of problems like magnetic energy storing causing high voltages at circuit breaking or other rapidly changing loads. Also magnetic and electrical EMC problems depending on internal and external crosstalk may occur. Another possible solution would be to design an active inductance. Active inductances have been made with bipolar transistors. Since bipolar transistors are current controlled devices, several are needed in some kind of high current gain configuration like Darlington connection to get the necessary high impedance to the control input of the circuit. Solutions like the one above is however complicated.

SUMMARY OF THE INVENTION

The present invention relates to a problem how to provide proper output load to a device under test requiring low resistance for DC voltages and high impedance for AC voltages.

A purpose with the invention is to facilitate measurements of a test object without essentially influencing superposed AC voltage parameters from the device under test.

The problem is solved by the invention by an active load arrangement comprising a voltage-controlled transistor associated with a feedback arrangement. The feedback arrangement controls the DC bias point, and by superimposed AC input the arrangement controls the phase and the amplitude for the control signals to the transistor inputs.

More in detail, the active load arrangement comprises a voltage-controlled transistor called Metal Oxide Semiconductor Field Effect Transistor, MOSFET, having a

source, a gate and a drain. The drain is connected to an input of the arrangement associated with an output of the object under test. A resistor is connected between the gate and the drain. An inductance is connected between the source and an output of the arrangement associated with an input of the object under test. A capacitance is connected between the gate and the arrangement output.

One advantage with the invention is that the impedance for the active load arrangement not is limited to the internal drain-source resistance but can be further enhanced by the feedback nets.

Another advantage with the invention is that high impedance is obtained without the need of bulky passive components.

Yet another advantage is that the MOSFET is a cheap component and only one active device with a few additional components are needed for the invention.

The invention will now be described more in detail with the aid of preferred embodiments in connection with the enclosed drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a schematic diagram of an active load arrangement connected to a test object.

Figure 2 shows an active load arrangement more in detail with the aid of an equivalent MOSFET diagram.

Figure 3 shows results from a simulation using the active load arrangement.

Figure 4 shows a schematic diagram of two active load arrangements connected in reverse.

DETAILED DESCRIPTION OF EMBODIMENTS

In figure 1 is disclosed a test arrangement TA comprising an active load arrangement Z connected to a test object TO. The active load arrangement provides proper output load to the object under test. The test object, which for example can be a POTS line interface circuit in a telecommunication system, comprises an object output O1 and an object input I1. The load arrangement Z comprises an arrangement input I2 associated with the object output O1. The arrangement Z also comprises an arrangement output O2 associated with the object input I1. The load arrangement Z further comprises a MOSFET with a drain D, a gate G and a source S. The semiconductor in this example is of the type IRF610. The drain D is connected to the arrangement input I2. A first resistance R1, in the example 2,2E6 ohm, is connected between the drain D and the gate G. A second resistance R2, in the example 2,2E6 ohm, is connected between the gate G and the source S. A capacitor C1, in the example 6,8μF, is connected between the gate and the arrangement output O2. An inductance L1, in the example 42mH, is connected between the source and the arrangement output O2. The inductance L1 is called a first feedback net FBN1 and the resistances R1 and R2 together with the capacitor C1 is called a second feedback net FBN2.

The test object TO in this example is a POTS line interface circuit and it works under normal OFF HOOK operation with an AC voltage superposed on a DC voltage. In order to activate and measure the AC parameters of the test object, a load arrangement called DC-loop is necessary to supply low-resistance DC load and high-impedance AC load. The low-resistance DC load make the line interface circuit to go into the state where it is working with 2 wire AC voice signals. The high-impedance AC-load is needed because the superposed AC parameters must be as uninfluenced as possible

by the DC load. The load arrangement must be essentially higher than the AC impedance of the test object TO.

The invention will now be explained with the aid of figure 1 and figure 2. Figure 2 discloses more in detail the active load arrangement Z shown in figure 1. Figure 2 shows the earlier mentioned first resistance R1, the second resistance R2 and the capacitor C1. In figure 2, also the internal resistance RL of the inductance L1 is shown. The MOSFET shown in figure 1 is shown in figure 2 as an equivalent circuit diagram suitable for simulation of the invention, i.e. a simulation model. A voltage controlled Current Source CS is situated in the MOSFET model between the gate G, the drain D and the source S. A static drain-to-source resistance R_{ds} is shown between drain and source. A reverse transfer capacitance C_{rss} is shown between the gate and the drain. To be able to simulate the approximate DC bias point of the circuit a voltage bias V_{bias} is placed between the source S and a minus pin of the voltage controlled current source CS.

A suitable working-point for the MOSFET is selected with respect to the DC needed for the test object TO, the reverse transfer capacitance C_{rss} and the power dissipation of the MOSFET. High drain D to source S voltage results in high power dissipation and low Crss. Low drain current results in high R_{ds}, low forward transconductance *Gfs* and low power dissipation. The working point is selected by means of the first resistance R1 and the second resistance R2. R1 and R2 will bias the gate so that the drain voltage will be approximately 10V and so that the gate voltage will be approximately 5V when using a MOSFET type IRF610 which has a V_{bias} of about 5V for the current values that are valid, i.e. 10-100mA. This bias will create sufficient drain-source voltage for different currents to the testobject. The

capacitor C1 together with the resistance R1 and R2 will have the effect of a low-pass filter. Since the MOSFET is a voltage controlled device it has a very high input resistance. R1 and R2 can then be set to very high resistance values without being loaded by gate currents. This is necessary because R1 and R2 add AC load to the circuit. C1 can be set to a low capacitance value while the circuit still will reach the necessary filtering capability, because R1 and R2 are high resistive. This is also an advantage because the low capacitance value eliminates the need of an electrolytic capacitor.

The superposed AC delivered from the test object will due to the low-pass filter R1, R2 and C2 cause the AC voltage on the gate G to go towards the object output O2.

R_{ds}, CS and L1 creates a signal path to the source S. The superposed AC will then result in a voltage across L1 which gives a source to gate voltage when the voltage between the gate and the output O2 goes towards zero which will rise the Z_{ds} above the R_{ds} value.

The AC behavioral of the MOSFET, somewhat simplified without the affection of C_{rss}, the impedance Z_{ds} between drain D and source S can be expressed in the following equation:

$$Z_{ds} = \frac{V_{ds}}{\frac{V_{ds}}{R_{ds}} + Gfs * V_{gs}}$$

V_{ds} is the AC voltage between drain and source.

R_{ds} is the linearized resistance between drain and source at a fixed DC current and voltage. IRF610 is typical 10kohm at DC drain current 80mA and DC drain to source voltage 10V.

V_{gs} is the AC voltage between gate and source.

Gfs is the linearized forward transconductance at a fixed DC current and voltage. IRF610 is typical 0.31 A/V at DC drain current 80mA and DC drain-source voltage 10V, for $V_{gs}=V_{ds}$ then $Z_{ds}=1/Gfs$. For IRF610 10V/80mA, Z_{ds}=3.2 ohm.

When the V_{gs} voltage goes towards zero it can be seen in the equation that drain-source impedance Z_{ds} goes towards R_{ds}, for IRF610 10V/80mA, Rds=10kohm.

If then V_{gs} is inverted and $V_{ds}/R_{ds}+Gfs*V_{gs}$ becomes zero, Z_{ds} is equal to infinity.

In the invention the feedback nets are arranged so that at low frequencies $V_{gs}=V_{ds}*R1/(R1+R2)$ applies. The low frequency AC impedance will then be low. At high freguencies the V_{gs} will change phase and amplitude in a way that the impedance rises and $V_{ds}/R_{ds}+Gfs*V_{gs}$ goes towards 0. When V_{gs} gets negative the impedance will be even higher than R_{ds}.

According to the invention, when the AC gate voltage goes towards zero, the AC drain current I_{drain} will decrease. Due to the R_{ds} and Gfs, a voltage U_L will arise over L1 and RL and an inverted gate-source voltage appears. As can be seen in the equation, the inverted gate-source voltage V_{gs} leads to increased drain-source impedance Z_{ds}, above R_{ds}. This appears distinctly in figure 3 where a simulation using the exemplified arrangement is presented.

In figure 3 is disclosed a simulation of the above described active load arrangement. It is to be observed that the simulation is disclosed schematic with a purpose to show the principle and enhance the understanding of the invention. In figure 3 can be seen three diagrams. A first diagram U shows

a voltage U_G between the gate G and the output O2, and a voltage U_S between the source S and the output O2, as a function of the frequency f. In a second diagram P_h the phase between the input I2 and the output O2 is shown as a function of the frequency f. A third diagram Z shows the I2 to O2 impedance as a function of the frequency f. In the first diagram U can be seen how the source voltage U_S and the gate voltage U_G decreases by increasing frequency f due to the two feedback nets FBN1 and FBN2. At a specific point $U_S=U_G$ applies. Because of phase differences of about fifty degrees between FBN1 and FBN2, U_{SG} is almost equal to U_S or U_G. At this point the I2 to O2 impedance Z is higher than R_{ds}. This can be seen in the third diagram where Z = 18kohm. At this point the drain to source impedance Z is equal to R_{ds}, as have been explained above. In the second diagram Ph the phase goes from approximately -100 degrees to + 100 degrees by increasing frequency, i.e. from inductive to capacitive impedance. When the phase curve reach zero degrees, the impedance reaches it maximum at the parallel resonance of the active load arrangement. The Z in the third diagram is resistive at DC and gradually goes inductive from low frequencies up to a point where it creates a parallel resonance circuit together with C_{rss}. R1 is in parallel with the circuit and limits the maximum impedance that can be reached because at high frequencies the reactance of C1 is much lower than the resistance of R1 and R2.

When the invention is to be used for measurement purposes it may be made for bipolar operation. The invention can be placed in a rectifier bridge on the rectified output side. The rectifier bridge add 2 reversed biased diodes with 2 diode capacitances and the other 2 forward biased diodes add

2 diode voltage drops and diode resistances to the invention.

A second embodiment is disclosed in figure 4. The figure shows a solution where two active load arrangements like the one shown in the first embodiment are connected in reverse and thus bypassed by an internal drain-source diode of one of the MOSFETs. By connecting the two arrangements reversed together and by slightly modify the solution they will be able to share the same inductance L1. This modification is disclosed in figure 4. A load arrangement Z1 comprises a second semiconductor MOSFET2 comprising a second source S2, a second gate G2 and a second drain D2. The second source S2 is connected via a fourth resistance R4 to the second gate G2. The second gate G2 is connected via a fifth resistance R5 to the second drain D2 and to an arrangement output O3. The second drain S2 is connected via the capacitance C1 discussed in the first embodiment, to the gate G. The second gate G2 is connected via a second capacitor to the source S of the earlier discussed MOSFET. The second source S2 is connected to the earlier mentioned impedance L1. Compared to the bipolar rectifier solution this gives no additional load capacitance and only one additional diode voltage drop. However this solution needs more DC bias point stabilisation time than the previous by changing polarity of the input.

Different variations are of course possible within the scope of the invention. The resistor R2 can for example be omitted if lower impedance depending on higher C_{rss} and a smaller signal before clipping can be accepted. R2 may be connected across C1 instead of between MOSFET gate-source. That will only slightly affect the DC bias voltage depending on the size of RL, which normally is made low to get low different DC voltages across the L1 inductor at different drain currents. The more the DC voltage to source-O2 changes, C1 needs more reloading time, which is not desirable. The

invention is not limited to the above described and in the drawings shown embodiments but can be modified within the scope of the enclosed claims.

CLAIMS

1. Active load arrangement (Z) used to provide output load to an object (TO) under test, which arrangement (Z) comprises a voltage controlled transistor (MOSFET) having a source (S), a gate (G) and a drain (D), which drain (D) is associated with the gate (G) and connected to an arrangement input (I2) associated with the object (TO), and which source (S) is connected to an arrangement output (O2) associated with the object *characterised by* a feedback arrangement connected to the source (S) and to the gate (G), which feedback arrangement by varying frequency changes phase and amplitude of the gate-to-source voltage to obtain low impedance at low frequencies and high impedance at high frequencies.

2. Active load arrangement according to claim 1, whereby the feedback arrangement comprises a first feedback net (FBN1) in which an inductance (L1) is connected between the source (S) and the arrangement output (O2).

3. Active load arrangement (Z) according to claim 2, whereby the feedback arrangement comprises a second feedback net (FBN2) in which a first resistance (R1) is connected between the gate (G) and the arrangement input (I2), and a second resistance (R2) is connected between the gate (G) and the source (S), and a capacitor (C1) is connected between the gate (G) and the arrangement output (O2).

4. Active load arrangement (Z) used to provide proper output load to an object (TO) under test, which arrangement (Z) comprises a voltage controlled transistor (MOSFET) having a source (S), a gate (G) and a drain (D), which drain is connected to an arrangement

input (I2) associated with an output (O1) of the object (TO), whereby a first resistance (R1) is connected between the gate (G) and the drain (D), *characterised in* that an inductance (L1) is connected between the source (S) and an arrangement output (O2) associated with an input (I1) of the object (TO), and that a capacitance (C1) is connected between the gate (G) and the arrangement output (O2).

5. Active load arrangement (Z) used to provide proper output load to an object (TO) under test according to claim 4, whereby a second resistance (R2) is connected between the gate (G) and the source (S).

6. Active load arrangement (Z) used to provide proper output load to an object (TO) under test according to claim 4, whereby a second resistance (R2) is connected in parallel with the capacitance (C1).

7. Active load arrangement (Z) used to provide proper output load to an object (TO) under test according to any of claim 4-6, whereby a rectifier bridge is situated between the test object (TO) and the test arrangement (TA).

8. Active load arrangement (Z1) used to provide output load to an object (TO) under test, comprising an active load arrangement (Z) according to any of claim 1-3 and a second voltage controlled transistor (MOSFET2) comprising a second source (S2), a second gate (G2) and a second drain (D2), which second source (S2) is connected via the feedback arrangement to the source (S) and the gate (G) and via a fourth resistor (R4) to the second gate (G2), which gate (G2) is connected via a fifth resistance (R5) to the second drain (D2) and to an arrangement output (O3) associated with the test object

(TO) and which second gate (G2) is connected to the source (S) via a second capacitor (C2).

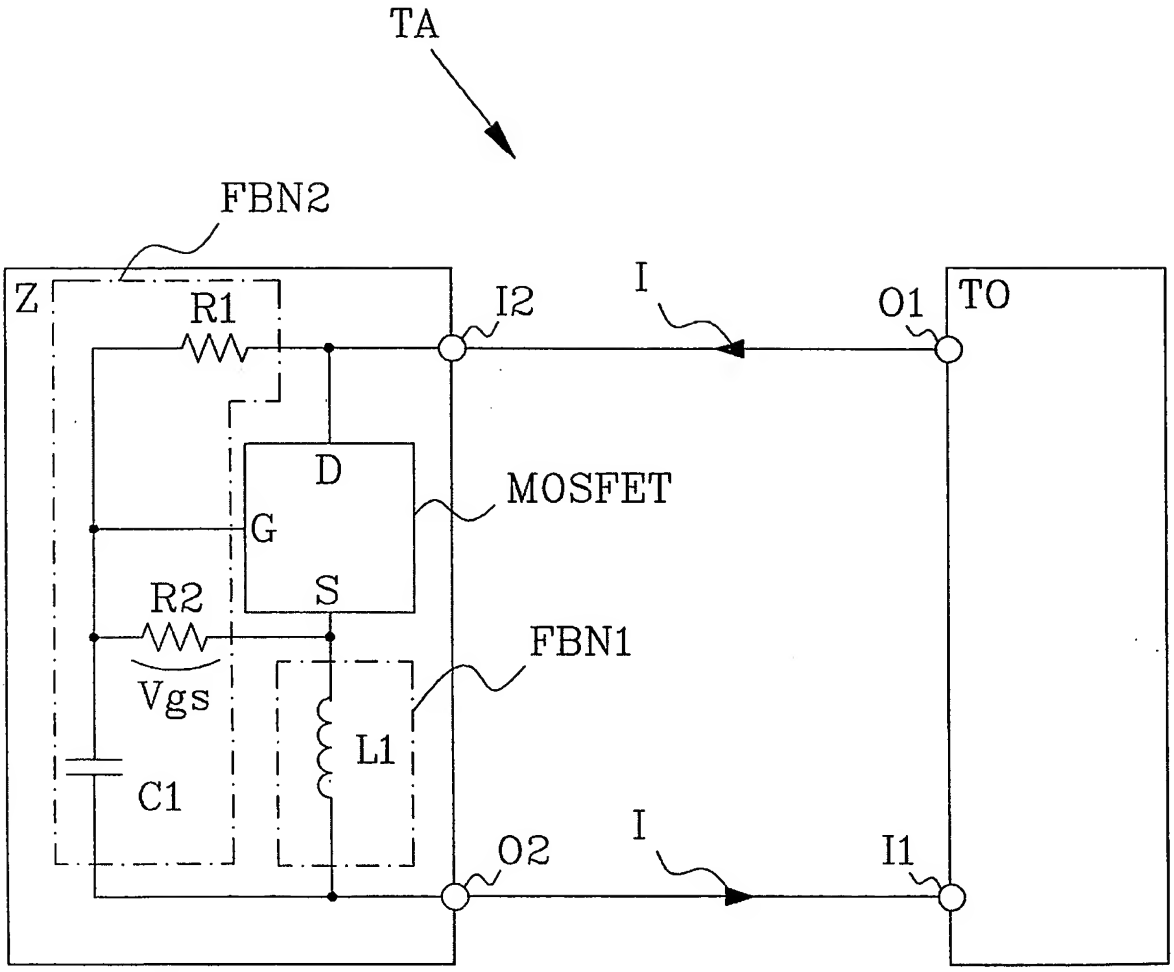
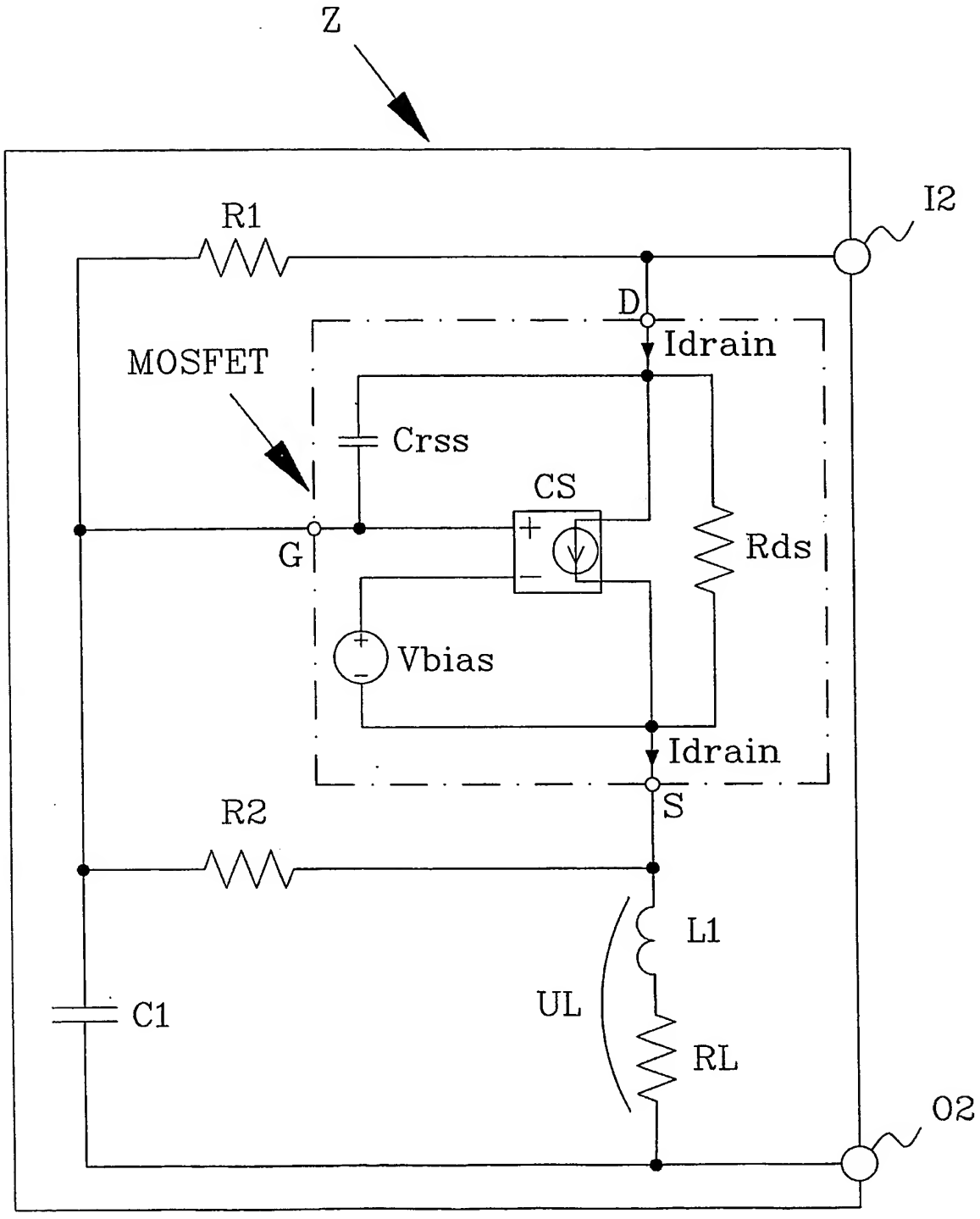


Fig. 1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R1
D
Idrain
MOSFET
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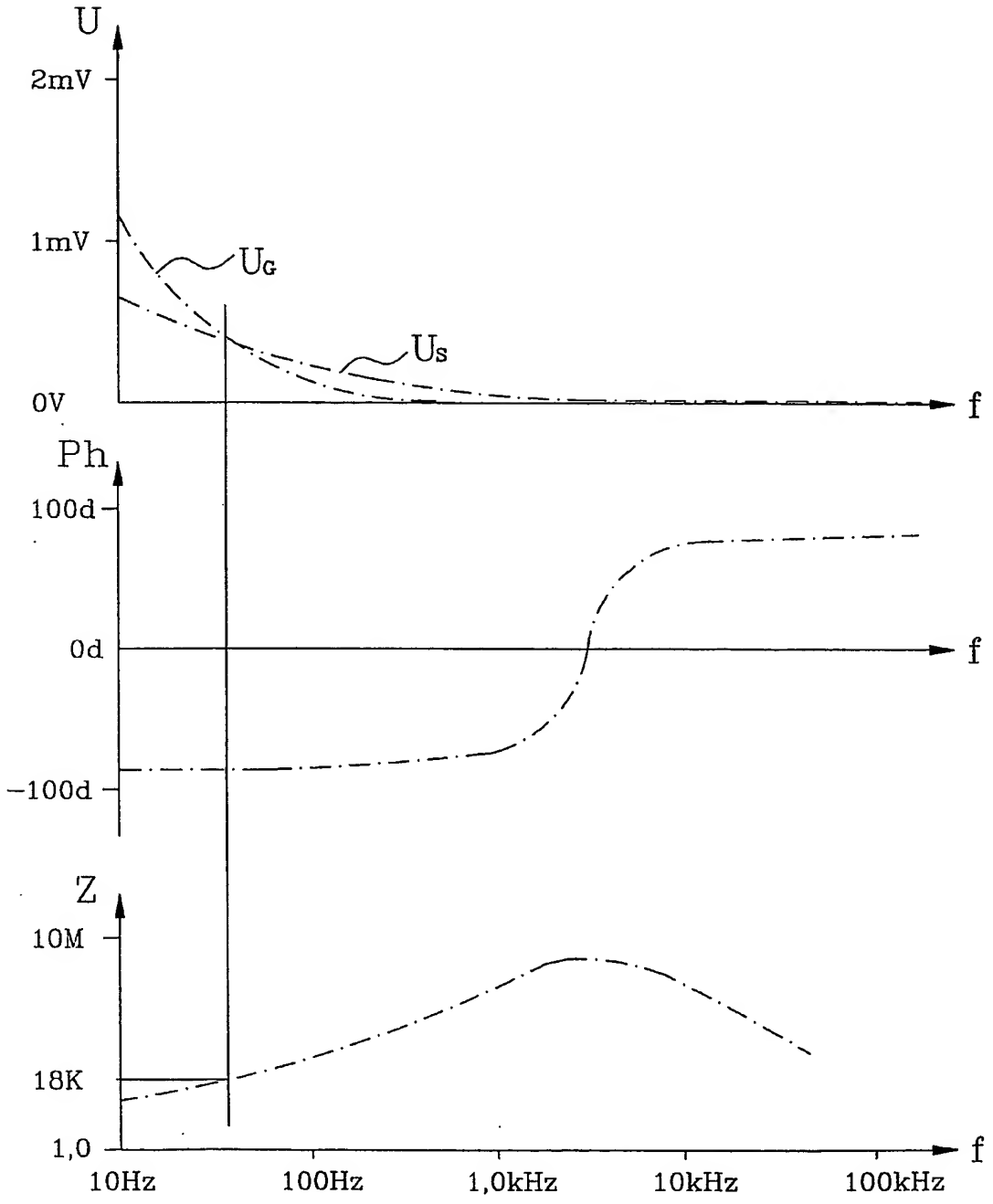
CS
G
Rds
Vbias
Idrain
S
R2
L1
C1
UL
RL
02

Fig. 2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1mV
0V
U_G
U_S
f
Ph
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0d
−100d
f
Z
10M
18K
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10Hz
100Hz
1,0kHz
10kHz
100kHz

Fig. 3

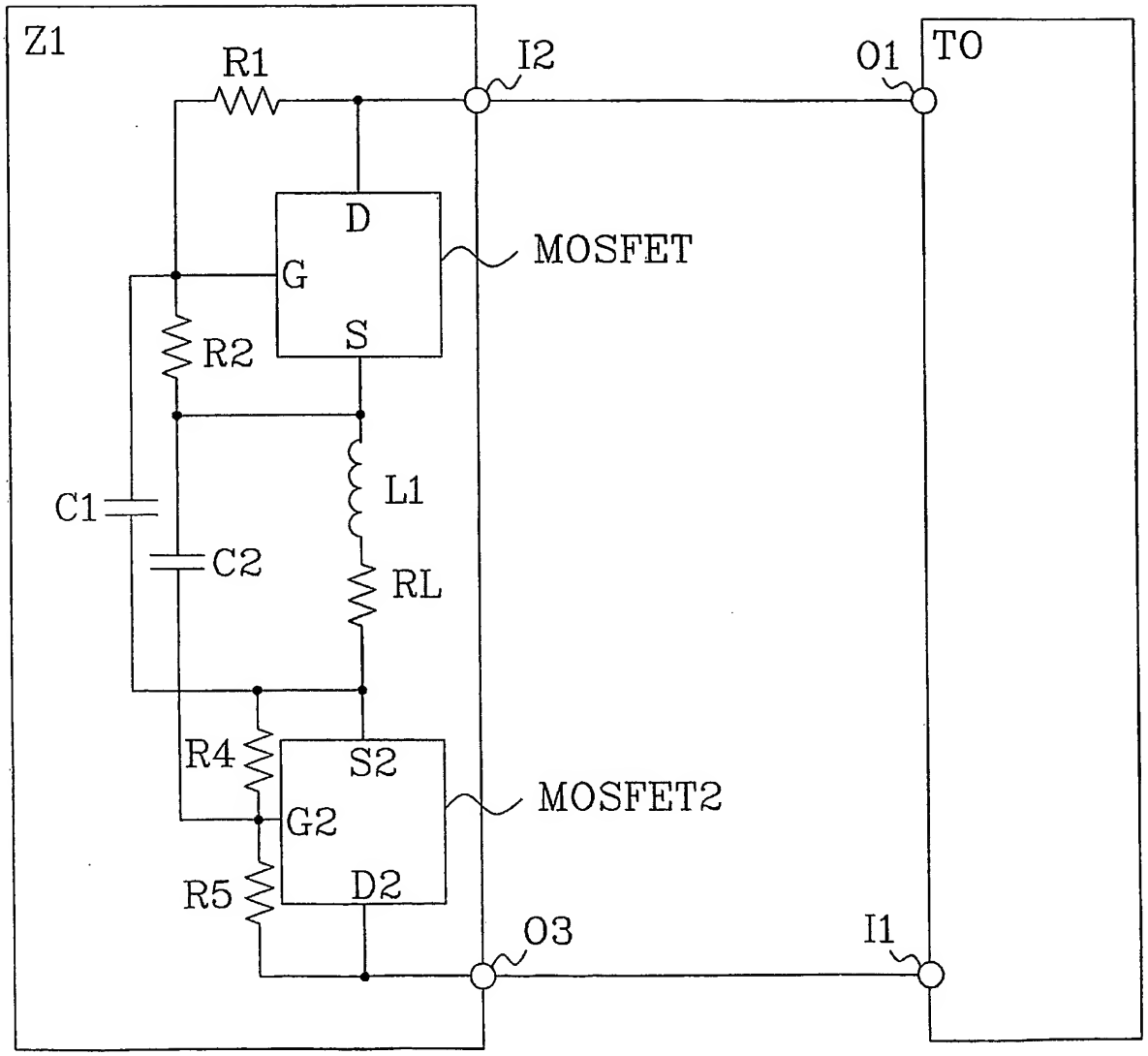
Z1
R1
I2
O1
TO
D
G
S
MOSFET
R2
L1
C1
C2
RL
R4
S2
G2
MOSFET2
R5
D2
O3
I1

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 02/01092

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H03H 11/46, H03F 3/60, G01R 31/02
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: G01R, H03F, H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	EP 0528413 A2 (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.), 24 February 1993 (24.02.93), column 6, line 27 - line 39, figure 2	1-8
X	WO 9705695 A1 (SCIENTIFIC-ATLANTA, INC.), 13 February 1997 (13.02.97), page 9, figure 6	1-8
A	US 5361038 A (BARRY R. ALLEN ET AL), 1 November 1994 (01.11.94), abstract	1-8

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
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Date of the actual completion of the international search	Date of mailing of the international search report
10 January 2003	16 -01- 2003
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Sture Elnäs/EÖ Telephone No. +46 8 782 25 00

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 02/01092

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Information on patent family members

30/12/02

International application No.
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